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PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10007300	11/08/2001	257	5	2811	THIEN TRAN

**APPLICANTS: Jono Keiji; Ueda Hirokazu; Watanabe Hiroyuki;

**CONTINUING DATA VERIFIED:

THIS APPLICATION IS A DIV OF 09/652,550 08/31/2000

YES TT

** FOREIGN APPLICATIONS VERIFIED:

NONE TT

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	

Foreign priority claimed	☐ yes ☑ no	ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☑ no	
Verified and Acknowledged Examiners's intials	TT	KM1-003

TITLE : Methods of forming an isolation trench in a semiconductor, methods of forming an isolation trench in a surface of a silicon wafer, methods of forming an isolation trench-isolated transistor

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED: Total Claims / Print Claim for O.G
ISSUE FEE: Amount Due / Date Paid	Primary Examiner	DRAWING: Sheets Drwg. / Figs.Drwg. / Print Fig.
☐ TERMINAL DISCLAMER	PREPARED FOR ISSUE	Applicati n Examiner

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